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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/294,341	04/20/1999	MASAAKI HIROKI	0756-1964	6027

31780 7590 10/05/2004

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EXAMINER	
LIANG, REGINA	

ART UNIT	PAPER NUMBER
2674	19

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/294,341	Applicant(s) HIROKI, MASAAKI	
	Examiner Regina Liang	Art Unit 2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12-17,19-23,25-35 and 37-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10,12-17,19-23,25-35 and 37-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *18*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3-6, 8, 10, 12, 33, 35, 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Okada et al (US. APT. NO. 5,734,378 hereinafter Okada).

As to claim 1, Fig. 1 of Okadata discloses a display device comprising a display panel having a switching element for every pixel electrode (inherent that each pixel of the display panel having a switching element such that a gate driver for controlling the gate of the switching element), a line driving circuit (a gate driver, col. 6, line 6), a signal line driving circuit (25, 27), a control circuit (23a) including a delay circuit (40 in Fig. 2) connected to the signal line driving circuit, a video signal processing circuit (23) connected to the control circuit (23a) and the signal line driving circuit (25, 27). Fig. 3 of Okada also discloses the delay circuit (40 in Fig. 2) produces a phase difference (ϕ) in a second signal (CK') with respect to a phase of a first signal (CK) which is input to the signal line driving circuit (see Fig. 3 and col. 7, lines 62-66).

As to claim 3, Okadata teaches each of the first signal and the second signal is a clock signal (synchronization clock CK, CK').

As to claims 4, 10, 35, Fig. 3 of Okadata shows that the fist signal (CK) has a different rise time period and a different signal fall time period from the second signal (CK').

As to claims 5, 12, Fig. 3 of Okadata also teaches that a signal rise time period or a signal fall time period of the first or second signal is shorter than a half of a signal holding time period of the first or second signal.

As to claims 6, 37, Fig. 3 of Okadata shows that the phase difference in the second signal produces a phase difference corresponding to a signal rise time period of the first signal.

As to claims 8, 33, note the discussion of claim 1 above. In addition, Fig. 3 of Okadata teaches each of the first signal and the second signal is a clock signal (synchronization clock CK, CK') and a signal rise time period or a signal fall time period of the first or second signal is shorter than a half of a signal holding time period of the first or second signal.

Claim Rejections - 35 USC § 103

4. Claims 39, 40, 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okadata.

Okadata discloses the claimed invention except for a length of the phase difference is at least a signal rise time period of the first signal or a signal fall time period of the first signal, and shorter than a half of a signal holding time period. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the display device of Okadata to have the length of the phase difference as claimed, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

5. Claims 7, 13, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okadata in view of Shimada (US. PAT. NO. 5,801,678 hereinafter Shimada).

Okadata teaches the display device including a transmission type LCD panel. Okadata does not disclose the display device is a projection type display device. However, Fig. 2 of Shimada teaches a LCD display device is a projection type display device having a light source (202) for projection. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the display device of Okadata to be a projection type display device as taught by Shimada so as to provide a projection type LCD device for projecting the images on the projection screen.

6. Claims 9, 14-17, 19, 21-23, 25, 27-31, 34, 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okadata in view of applicant's admitted prior art (Fig. 5 and page 1, line 10, to page 4, line 5 of the specification).

As to claims 9, 15, 22, 27, 34, Okadata does not disclose the first signal has a reversed phase relation with the second signal. However, Fig. 5 of the admitted prior art teaches a first clock signal has a reversed phase relation with a second clock signal. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the display device of Okadata to comprise the first signal having a reversed phase relation with the second signal as taught by the admitted prior art such that the resolution of a display image is improved.

As to claims 14, 21, Okadata does not disclose the first signal and the second signal are input to a same shift register circuit. However, Okadata discloses the first signal and the second signal are inputted to the signal line driving circuit (both clock signals CK and CK' are inputted to the signal line driving circuit 25a and 27a as shown in Fig. 5). The admitted prior art teaches a signal line driving circuit of a display device comprising a shift register circuit and a latch circuit, and the first clock signal and the second clock signal are inputted to a shift register circuit (page 3, lines 5-6 of the admitted prior art). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the signal line driving circuit of Okadata to have a shift register circuit or a latch circuit and both the first signal and the second signal are inputted to the shift register circuit or the latch circuit as taught by the admitted prior art so as to control the data shifting in the signal line driving circuit for driving the data lines of the display device such that a high quality image can be realized.

As to claims 16, 28, Okadata teaches each of the first signal and the second signal is a clock signal (synchronization clock CK, CK').

As to claims 17, 23, 29, Fig. 3 of Okadata shows that the fist signal (CK) has a different rise time period and a different signal fall time period from the second signal (CK').

As to claims 19, 25, 31, Fig. 3 of Okadata shows that the phase difference in the second signal produces a phase difference corresponding to a signal rise time period of the first signal.

As to claim 30, Fig. 3 of Okadata also shows that a signal rise time period or a signal fall time period of the first or second signal is shorter than a half of a signal holding time period of the first or second signal.

As to claims 41-43, Okadata as modified by the admitted prior art does not discloses a length of the phase difference is at least a signal rise time period of the first signal or a signal fall time period of the first signal, and shorter than a half of a signal holding time period. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the display device of Okadata as modified by the admitted prior art to have the length of the phase difference as claimed, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

7. Claims 20, 26, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okadata and the admitted prior art as applied to claims 14, 21, 27 above, and further in view of Shimada.

Okadata teaches the display device including a transmission type LCD panel. Okadata as modified by the admitted prior art does not disclose the display device is a projection type display device. However, Fig. 2 of Shimada teaches a LCD display device is a projection type display device having a light source (202) for projection. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the display device of Okadata as modified by the admitted prior art to be a projection type display device as taught by Shimada so as to provide a projection type LCD device.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 3-10, 12-17, 19-23, 25-35, 37-44 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takabayashi et al (US. PAT. N O. 6,320,572) teaches a control circuit for LCD having a delay circuit.

Hiroki (US. PAT. NO. 6,628,253) teaches a display device and method of driving the same.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (703) 305-4719. The examiner can normally be reached on Monday-Friday from 9AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

REGINA LIANG
PRIMARY EXAMINER
ART UNIT 2674

RL
9/30/04